WHAT IS CLAIMED IS

1. A semiconductor device comprising:

a BGA substrate having one principal plane furnished with a large number of solder balls, said solder balls constituting a ball grid array;

a semiconductor chip mounted on another principal plane of said BGA substrate, said semiconductor chip being electrically connected to said BGA substrate by metal wires; and

chip capacitors mounted on said semiconductor chip to reduce power source noise.

2. A semiconductor device comprising:

a BGA substrate having one principal plane furnished with a large number of solder balls, said solder balls constituting a ball grid array;

a first semiconductor chip including bumps and active regions formed on the same side as said bumps, said bumps serving as electrodes attached to said one principal plane of said BGA substrate; and

a first chip capacitor attached to said active regions of said first semiconductor chip or to the opposite side of said active regions of said first semiconductor chip, said first chip capacitor serving to reduce power source noise.

3. The semiconductor device according to claim 2, wherein said first semiconductor chip further includes through-type via contacts extending from said active regions to said opposite side in said first semiconductor chip, and said first chip capacitor is electrically connected to said active regions through said through-type via contacts.

4. The semiconductor device according to claim 2, further comprising:

a second semiconductor chip mounted on said opposite side of said active regions of said first semiconductor chip, said second semiconductor chip being electrically connected to said BGA substrate by metal wires; and

a second chip capacitor attached to said second semiconductor chip as well as a first chip capacitor attached to

said active region of said first semiconductor chip, said second chip capacitor serving to reduce power source noise.

5. The semiconductor device according to claim 1, further comprising:

a conductive radiator attached to said another principal plane of said BGA substrate, said conductive radiator covering said semiconductor chip; and

a shield plane incorporated in said BGA substrate, said shield plane constituting a shield of said semiconductor chip in combination with said conductive radiator;

wherein said conductive radiator and said shield plane are connected to ground potential.

6. The semiconductor device according to claim 2, further comprising:

a conductive radiator attached to said another principal plane of said BGA substrate, said conductive radiator covering said first semiconductor chip; and

a shield plane incorporated in said BGA substrate, said shield plane constituting a shield of said first semiconductor chip in combination with said conductive radiator;

wherein said conductive radiator and said shield plane are connected to ground potential.

7. The semiconductor device according to claim 6, further comprising a heat transfer member interposed between said opposite side of said active regions of said semiconductor chip and said conductive radiator.

8. The semiconductor device according to claim 5, further comprising a radiating fin attached to an external surface of said conductive radiator.

9. The semiconductor device according to claim 6, further comprising a radiating fin attached to an external surface of said conductive radiator.

10. A semiconductor device comprising:

a semiconductor chip including bumps and active regions,

said bumps serving as electrodes and being formed on one principal plane of said semiconductor chip, said active region being formed on the opposite side as said bumps;

wherein chip capacitors can be attached to said active regions of said semiconductor chip, and said chip capacitors are served to reduce power source noise.

11. The semiconductor device according to claim 10, further comprising a BGA substrate having one principal plane furnished with a large number of solder balls, said solder balls constituting a ball grid array;

wherein said semiconductor chip is attached to said one principal plane of said BGA substrate by means of said bumps.

12. The semiconductor device according to claim 10, wherein said semiconductor chip further has through-type via contacts extending from said active regions to a bump mounting surface thereof in said semiconductor chip, and said through-type via contact is served to ensure electrical connection between said active regions and said bumps.

13. The semiconductor device according to claim 10, further comprising:

a system substrate;

a plurality of mounting pads furnished on one principal plane of said system substrate, said plurality of mounting pads being electrically connected to said bumps of said semiconductor chip;

chip capacitors mounted either on said one principal plane of said system substrate or on a back thereof, said chip capacitors serving to reduce power source noise; and

a sealing resin member for sealing said semiconductor chip.

14. The semiconductor device according to claim 13, further comprising a plurality of rework mounting pads furnished on said one principal plane of said system substrate in contiguous to said mounting pads.

15. The semiconductor device according to claim 13,

further comprising a plurality of semiconductor chips layered on said semiconductor chip, each of said layered semiconductor chips including active regions on one surface thereof, bumps on another surface thereof, and a through-type via contacts extending from said one surface to said another surface in said semiconductor chips, said active regions and said bumps being electrically connected through said through-type via contacts.